CLMPTO
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CM.

1. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said bit line contact feature is characterized by a contact hole bounded by insulating side walls; and

said contact hole is partially filled with a conductively doped polysilicon plug defining an upper plug surface profile at least a portion of which is substantially convex.

2. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said bit line contact feature is characterized by a contact hole bounded by insulating side walls; and

said contact hole is completely filled with a conductively doped polysilicon plug defining an upper plug surface profile at least a portion of which is substantially convex.

CLAIMS 3-12. (CANCELLED)

13. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is partially filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially convex; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

14. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is completely filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially convex; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

CLAIMS 15-22. (CANCELLED)

23. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a contact hole;

said polysilicon plug partially fills said contact hole; and

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line.

24. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a contact hole;

said polysilicon plug completely fills said contact hole; and

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line.

CLAIMS 25-32. (CANCELLED)

33. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a first contact hole bounded by insulating side walls;

said polysilicon plug partially fills said first contact hole;

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line;

said charge storage structure further comprises a storage node including a conductively doped polysilicon plug formed within a second contact hole bounded by insulating side walls;

said polysilicon plug partially fills said second contact hole; and

said doped polysilicon plug of said storage node defines an upper plug surface profile that is substantially convex.

34. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a first contact hole bounded by insulating side walls;

said polysilicon plug completely fills said first contact hole;

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line;

said charge storage structure further comprises a storage node including a conductively doped polysilicon plug formed within a second contact hole bounded by insulating side walls;

said polysilicon plug completely fills said second contact hole; and

said doped polysilicon plug of said storage node defines an upper plug surface profile that is substantially convex.

CLAIMS 35-41. (CANCELLED)

42. A semiconductor device comprising:

a substrate having a first active area formed therein;

at least one insulating layer over said substrate;

a conductive line over said at least one insulating layer;

a contact configured to couple said conductive line to said active area, said contact characterized by:

a contact hole formed through said at least one insulating layer, said at least one insulating layer defining insulating sidewalls; and,

a conductive plug formed within said contact hole, said conductive plug having a substantially convex upper plug surface profile, wherein at least said upper plug surface profile is defined by a doped polysilicon, and wherein said conductive plug completely fills said contact hole.

43. A semiconductor device comprising:

a substrate having a first active area formed therein;

at least one insulating layer over said substrate;

a conductive line over said at least one insulating layer;

a contact configured to couple said conductive line to said active area, said contact characterized by:

a contact hole formed through said at least one insulating layer, said at least one insulating layer defining insulating sidewalls; and,

a conductive plug formed within said contact hole, said conductive plug having a substantially convex upper plug surface profile, wherein at least said upper plug surface profile is defined by a doped polysilicon, and wherein said conductive plug partially fills said contact hole.

CLAIM 44. (CANCELLED)